In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

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1. (Currently Amended) A digital processing system having a microprocessor, wherein the microprocessor comprises:

fetch circuitry for fetching instruction fetch packets from sequential memory address locations, wherein each fetch packet contains a first plurality of instructions, each instruction including an instruction type and a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction;

a second plurality of functional units, each of the second plurality of functional units operable to execute a ~~second plurality of instructions~~ corresponding instruction in parallel with other functional units, and

dispatch circuitry connected to said fetch circuitry and said second plurality of functional units operable to

select an execution packet from one or more fetch packets, wherein an execute packet varies in size and contains only a set of instructions that can be executed in parallel on the plurality of functional units, ~~whereby a first execute packet contains a different number of instructions than a second execute packet due to resource constraints~~ by scanning instructions from lower memory address locations to higher memory address locations adding an instruction to said execute packet when said p-bit of a prior instruction has said first digital state until said p-bit of an instruction has said second digital state, and

dispatch each instruction of said selected execute packet to a functional unit corresponding to said instruction type of said instruction.

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2. (Original) The digital processing system of Claim 1, wherein the first plurality is equal in number to the second plurality.

Claim 3 (Cancelled)

4. (Currently Amended) The digital processing system of Claim ~~3~~ 2, wherein the dispatch circuitry comprises:

a first latch to hold ~~the~~ said first plurality of instructions of a first fetch packet;

a second latch to hold ~~the~~ said first plurality of instructions of a second fetch packet immediately following said first fetch packet;

~~selection circuitry to select a first portion of the first execute packet from the first latch and a second portion of the first execute packet from the second latch~~

a first plurality of multiplexers, each multiplexer having a first input receiving an instruction from a predetermined position of said first latch, a second input receiving an instruction from a corresponding position of said second latch, a control input and an output, each multiplexer selecting at said output said instruction from said first latch, said instruction from said second latch or no instruction dependent upon said control input;

a dispatch control circuit connected to said first latch, said second latch and said plurality of multiplexers, said dispatch control circuit receiving said predetermined p-bit from each instruction of said first latch and each instruction of said second latch for control of said plurality of multiplexers via said

control inputs according the execute packets determined by said p-bits; and

a cross point circuitry connected to said plurality of multiplexers for dispatching said instructions at said output of said multiplexers to a functional unit corresponding to said instruction type of each instruction.

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Claims 5 and 6 (Canceled)

7. (Currently Amended) A method of operating a digital system having a microprocessor, wherein the microprocessor has a plurality of functional units for executing instructions in parallel, comprising the steps of:

storing instructions at sequential memory address locations, each instruction including an instruction type and a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction;

fetching a sequence of instruction fetch packets, wherein each fetch packet contains a first plurality of instructions;

~~examining~~ scanning the p-bit of each instruction of each fetch packet from lowest memory address location to highest memory address location to determine an ~~execution~~ execute packet ~~boundary~~ dependent on the p-bits;

~~selecting a first portion of an execute packet from a first fetch packet and a second portion of a first execute packet from a second fetch packet if the first execute packet boundaries span the first fetch packet and the second fetch packet~~

dispatching each instruction within the determined execute packet to one of a second plurality of execution units dependent upon an instruction type of the instruction.

8. (New) The method of Claim 7, wherein:

the first plurality of instructions in a fetch packet equals the second plurality of functional units.

9. (New) The method of Claim 7, wherein:

said step of determining an execute packet boundary dependent upon the p-bits includes

storing a first fetch packet in a first latch,

storing a second fetch packet in a second latch,

selecting an instruction from said first latch, a corresponding instruction from said second latch or no instruction dependent upon said p-bit from each instruction of said first latch and each instruction of said second latch.

10. (New) A digital processing system having a microprocessor, wherein the microprocessor comprises:

fetch circuitry for fetching instruction fetch packets from sequential memory address locations, wherein each fetch packet contains a first plurality of instructions, each instruction including an indication of a corresponding functional unit and an indication of an execute packet;

a second plurality of functional units, each of the second plurality of functional units operable to execute a corresponding instruction in parallel with other functional units, and

dispatch circuitry connected to said fetch circuitry and said second plurality of functional units operable to

select an execute packet from one or more fetch packets, wherein an execute packet varies in size and contains only a set of instructions that can be executed in parallel on the plurality of functional units, by scanning instructions from lower memory address locations to higher memory address

locations adding an instruction to said execute packet dependent upon said indication of an execute packet, wherein upon a branch into the middle of an execute packet not selecting instructions having memory address locations lower than the branch, and

dispatching each instruction of said selected execute packet to a corresponding functional unit.

11. (New) A method of operating a digital system having a microprocessor, wherein the microprocessor has a plurality of functional units for executing instructions in parallel, comprising the steps of:

storing instructions at sequential memory address locations, each instruction including an indication of a corresponding functional unit and an indication of an execute packet;

fetching a sequence of a first plurality instruction fetch packets, wherein each fetch packet contains a first plurality of instructions;

scanning the indication of execute packet of each instruction of each fetch packet from lowest memory address location to highest memory address location to determine an execute packet, wherein upon a branch into the middle of an execute packet not selecting instructions having memory address locations lower than the branch;

dispatching each instruction within the determined execute packet to a corresponding execution unit.